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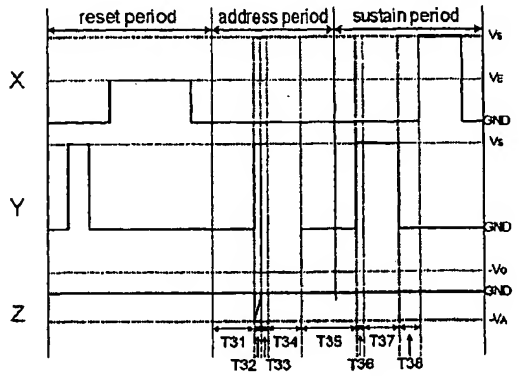
(54) Title: DRIVING METHOD FOR FAST ADDRESSING TECHNIQUE IN AN AC-PDP



(57) Abstract: The present invention relates generally to a method of driving alternating current plasma display panel and, more particularly, to a driving method, in which in an address period, a discharge initiating pulse and a wall charge accumulating pulse are applied to a scan electrode and an address pulse having an interval superposed on the discharge initiating pulse is applied to an address electrode, so that the width of the address pulse required for an address process is considerably reduced, thus being capable of performing high-speed addressing. The present invention provides a method of driving an Alternating Current (AC) Plasma Display Panel (PDP) in an address period to write image data, the AC PDP having a plurality of discharge cells for implementing images and a plurality of scan and address electrodes (Y and Z) for controlling the discharge cells, including, for a first line, a) an address discharge initiating step of initiating a discharge by applying a discharge initiating scan pulse to a scan electrode according to the image data, and an address pulse having a polarity opposite to that of the discharge initiating scan pulse to an address electrode while the scan pulse is applied; and b) a wall charge accumulating step of applying a wall charge accumulating scan pulse having a polarity opposite to that of the discharge initiating scan pulse and voltage size and width adjustable according to a number of wall charges desired to be accumulated.

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DRIVING METHOD FOR FAST ADDRESSING TECHNIQUE IN AN AC-PDP

Technical Field

The present invention relates generally to a method of driving alternating current plasma display panel and, more particularly, to a driving method, in which in an address period, a discharge initiating pulse and a wall charge accumulating pulse are applied to a scan electrode and an address pulse having an interval superposed on the discharge initiating pulse is applied to an address electrode, so that the width of the address pulse required for an address process is considerably reduced, thus being capable of performing high-speed addressing.

Background Art

FIG. 1a is a perspective view of a conventional Alternating Current (AC) type surface-discharge Plasma Display Panel (PDP) with front and back substrates thereof separated from each other, and FIG. 1b is a plan view of the conventional AC PDP. Referring to the drawings, an AC type surface-discharge PDP includes a front substrate 1, and a back substrate 2 adapted to have the same area as the front substrate 1 and positioned in parallel with the front substrate 1.

The front substrate 1 includes a plurality of sustain electrode lines X and Y each consisting of a transparent electrode 6 and a bus electrode 7 of low resistivity to apply voltage waveforms, a dielectric layer 8 formed among the sustain electrode lines X and Y to restrict a discharge current, and a protective layer 9 formed on the dielectric layer 8 to protect sustain electrode lines X and Y. The back substrate 2 includes a plurality of partition walls (or "barrier ribs") 3 for constituting a plurality of discharge spaces, a plurality of address electrode lines 4 positioned between the partition walls 3 to be perpendicular to the sustain electrode lines X and Y, and a fluorescent film 5 formed on the side and bottom

surfaces of the discharge spaces to cover the address electrode lines 4 to receive Vacuum UltraViolet (VUV) rays generated during a discharge and emit visible rays.

FIG. 2a is an entire driving waveform chart showing waveforms applied to the electrode lines X, Y and Z for a sub-field in a conventional AC PDP. FIG. 2b is an enlarged waveform chart that is plotted for a reset period, an address period, and a period for which a single sustain pulse is applied. FIG. 2c is a diagram showing the behavior of discharges and wall charges during respective periods divided in the enlarged waveform chart of FIG. 2b.

A detailed description is made with reference to the drawings. FIG. 2a illustrates an example of voltage waveforms that are applied to the sustain electrode lines X and Y each consisting of the transparent and bus electrodes 6 and 7 of FIG. 1 and the address electrode lines 4. In terms of periods, the total period may be divided into a reset period, an address period and a sustain period. In the reset period, a pulse having the same voltage as a sustain pulse and being narrower than the sustain pulse and a pulse having a voltage lower than the sustain pulse and being wider than the sustain pulse are alternately applied to the sustain electrode lines X and Y as shown in FIG. 2a so that the non-uniform state of wall charges generated while the AC PDP displays previous information are made uniform over the entire panel. In the address period, only target cells are addressed using a voltage difference between the one side sustain electrode lines X, that is scan electrodes, and the address electrode lines Z in such a way as to stack wall charges after an address discharge. In the sustain period, visible rays are emitted from the cells addressed in the address period by applying an alternating voltage to the both side sustain electrode lines X and Y, so that information is displayed.

The internal states of a discharge space during the respective periods are described with reference to FIGS. 2b and 2c. T11 is an interval that exhibits the internal state of the discharge space after reset pulses have been applied to the electrodes in a preceding reset period. In this interval following the reset period,

wall charges hardly exist in the inside of the discharge space, or wall charges are uniformly distributed over the panel. T12 is an interval in which an address discharge is generated due to the voltage difference between the scan electrode Y and the address electrode Z. In this interval, as charges of a polarity opposite to that of the voltages applied to the scan and address electrodes Y and Z begin to be accumulated at the same time that an address discharge starts, the intensity of an electric field actually applied to the discharge space is reduced, thus extinguishing the address discharge. T13 is an interval in which wall charges are produced using an electric field generated by a voltage difference between the scan electrodes Y and the address electrodes Z. In this interval, space charges existing for a certain period after the extinguishments of the address discharge are accumulated under the scan and address electrode Y and Z. T14 is an interval that exhibits the internal state of the discharge space after the address discharge and the accumulation of wall charges. In this interval, after voltages applied to the electrodes to generate the address discharge die out, the accumulated wall charges maintain the state thereof in which the wall charges are accumulated under the electrodes. T15 is an interval in which a sustain pulse is applied through the sustain electrode X so that a sustain discharge is generated. When a voltage of the same polarity as that of the accumulated wall charges is applied between two sustain electrodes X and Y, the sum of the applied voltage and a voltage resulting from the wall charges is actually applied to the discharge space, so that the sustain discharge is generated and charges of a polarity opposite to that of the applied voltage begin to be accumulated, thus reducing the intensity of an electric field applied to the inside of the discharge space and, therefore, extinguishing the discharge. T16 is an interval in which space charges are converted into wall charges using an electric field generated by the voltage difference between the two sustain electrodes X and Y. In this interval, the space charges that exist after the discharge has been extinguished are allowed to be accumulated under the two sustain electrodes X and Y. T17 is an interval that exhibits the internal state of the discharge space after the sustain discharge

and the accumulation of the wall charges. In this interval, after voltages applied to the electrodes to generate the sustain discharge die out, the accumulated wall charges maintain the state thereof in which the wall charges are accumulated under the electrodes, and will be used for the next discharge.

The wall charges accumulated in T13 of FIG. 2b are caused by the electric field resulting from the voltage difference between the scan electrode Y and the address electrode Z, and are mainly accumulated under the scan electrode Y and the address electrode Z. In contrast, the sustain discharge generated in T15 is generated by the voltage difference between the two sustain electrodes X and Y, so that the wall charges accumulated under the address electrode Z in T13 do not contribute to the sustain discharge of T15 and a first sustain discharge becomes weaker than later sustain discharges. To overcome these problems, various schemes have been proposed.

In the meantime, since the sufficient accumulation of wall charges is required for the stable generation of a discharge after the address period, the pulse applied between the scan electrode Y and the address electrode X in T12 and T13 of FIG. 2b requires a width of more than about 3 μm to accumulate the corresponding accumulation of the wall charges. Additionally, in the address process of the address period, addressing is performed using a discharge generated by the application of an address pulse through the address electrode Z on a scan line designated by the application of a scan pulse to the scan electrode Y, so that the address pulse cannot address a plurality of scan lines at the same time and the time required to address a single scan line is equal to or more than 3 μm. As a result, the time required to address the entire panel in a single sub-field is the product of the horizontal resolution of the panel and the time required to address the single scan line. For example, in the case of a PDP having Video Graphics Array (VGA)-level resolution (640×480), 480×3 μs=1.44 ms is required.

FIG. 3a is a diagram showing waveforms applied for a single TeleVision (TV) field (16.67 ms) during the driving of the conventional PDP with respect to

respective periods. FIG. 3b is a diagram showing times required for respective periods for a single TV field. A general case consists of eight sub-fields and each of the sub-fields is designated to exhibit a brightness of 1, 2, 4, 8, 16, 32, 64 or 128, so that a total of 256 brightnesses ranging from 0 to 255 can be obtained by the combination of various sub-fields. Further, a single sub-field consists of a reset period, an address period and a sustain period. When a general PDP having VGA-level resolution is driven, the time required for the reset period is about 1.44 ms in a single sub-field, the time required for the address period is about 1.44 ms and the time required for the sustain period is 10 μs to 1.28 ms according to a designated brightness. Accordingly, as shown in FIG. 3b, the reset period occupies 14% in a single TV field, the address period occupies 69%, and the sustain period occupies 17%, so that a light emission period is very short compared to the entire period and, therefore, this short light emission period considerably influences a reduction in the luminance of the PDP. When a PDP having Extended Graphics Array (XGA)-level resolution (1024×768) corresponding to a High Definition TV (HDTV) is driven, the time required for the reset period is about 300 μs and the time required for the address period is 768×3 μs=2.304 ms in a single sub-field, so that the sum of the times required for the reset and address periods is 20.382 ms in a single TV field and exceeds a single TV field time of 16.67 ms. Accordingly, a light emitting period cannot exist, and the driving of the PDP is impossible. There are many cases where sub-fields of a number more than eight are employed in a single TV field to reduce problems in image quality generated in a general PDP. In these cases, the light emission period is further reduced. The reduction of the above-described problems can be achieved by reducing the time required for the address period through high-speed addressing. Accordingly, various methods for such high-speed addressing have been proposed.

Of the methods for the high-speed addressing of an AC PDP, there are a driving method of performing an address discharge in a sustain period, a method in which each address electrode of a PDP is divided into upper and lower

electrodes, a driving method using a priming effect, and a multi-block scan method. In the driving method of performing an address discharge in a sustain period, a reset period, an address period and a sustain period are not divided from each other, and sustain discharges are performed on the remaining scan lines while an address process is performed on a designated scan line. However, this method is problematic in that when a sustain discharge is generated on a different line, an address pulse is applied to an address electrode placed across a plurality of lines, so that the driving of the PDP becomes unstable. In the method in which each address electrode of a PDP is divided into upper and lower electrodes, the address electrode is physically divided into two halves and an upper side line and a lower side line are simultaneously addressed, so that the time required for the address period is reduced to 1/2. However, this method is problematic in that double address circuits are required. The driving method using a priming effect is the method that causes the rapid generation of a discharge and reduces the width of an address waveform in such a way as to produce metastable particles in a discharge space by generating a strong discharge prior to an address process. The problem of this method is that unnecessary light emission is generated due to the strong discharge to generate metastable particles, thus reducing color contrast, and the number of metastable particles is reduced as time elapses, thus causing the address discharges on upper and lower lines to be different. The multi-block scan method is the method in which a PDP is divided into various blocks over the upper and lower parts thereof and reset, address and sustain periods are separated from each other in each block, and reset and address processes are performed in different blocks while a sustain discharge is generated in a block. However, this method is also problematic in that when a sustain discharge is generated on a different line, an address pulse is applied to an address electrode placed across a plurality of lines, so that the driving of the PDP becomes unstable.

Disclosure of the Invention

Accordingly, the present invention has been made keeping in mind the above problems occurring in the prior art, and an object of the present invention is to provide a method of driving an AC PDP, in which the time for which a designated scan line occupies an address electrode is minimally reduced and the time required to address an entire panel is reduced by dividing a discharge initiating interval and a wall charge accumulating interval using two scan pulses in the address period, so that a light emission time is lengthened in a single TV field, thus providing the effects in which the luminance of the AC PDP is improved, the AC PDP having XGA-level resolution can be allowed to be stably driven without changing the structure thereof, and reduced luminance due to the reduction of the light emission time can be compensated for when the number of sub-fields is increased to improve image quality.

In more detail, the present invention proposes driving waveforms in which in an address period, a discharge initiating pulse having a width narrower than that of a conventional single pulse and a wall charge accumulating pulse having a polarity opposite to that of the discharge initiating pulse and a width wider than that of the discharge initiating pulse are continuously applied to a scan electrode of a line on which a scan process is performed, and, at the same time, an address pulse having an interval superposed on the narrow discharge initiating pulse is applied to an address electrode for generating an address discharge. When these waveforms are employed, it is possible that the address time required on a designated scan line is reduced to the time corresponding to the width of a narrow discharge initiating pulse and, accordingly, high-speed addressing is enabled by considerably reducing the address periods of the entire panel, so that the time ratio occupied by a sustain period in a single TV field is relatively increased, thus increasing the overall luminance of the panel and being capable of compensating for luminance when sub-fields are divided to improve image quality.

In order to accomplish the above object, the present invention provides a method of driving an AC PDP in an address period to write image data, the AC PDP having a plurality of discharge cells for implementing images and a plurality of scan and address electrodes (Y and Z) for controlling the discharge cells, including, for a first line, a) an address discharge initiating step of initiating a discharge by applying a discharge initiating scan pulse to a scan electrode according to the image data, and an address pulse having a polarity opposite to that of the discharge initiating scan pulse to an address electrode while the scan pulse is applied; and b) a wall charge accumulating step of applying a wall charge accumulating scan pulse having a polarity opposite to that of the discharge initiating scan pulse and voltage size and width adjustable according to a number of wall charges desired to be accumulated.

Preferably, the wall charge accumulating scan pulse may have a voltage lower than the discharge initiating scan pulse.

Preferably, the wall charge accumulating scan pulse may be applied when a certain pause period elapses after the application of the discharge initiating scan pulse.

Preferably, the method may further include the step of maintaining a certain voltage on a common sustain electrode (X) during a partial interval of the address period.

Preferably, the method may further include the step of generating a full-scale address discharge in a reset period prior to the address period to reduce necessary voltage of pulses applied to the electrodes in the address period.

Preferably, the discharge initiating scan pulse may have a positive voltage with respect to a reference potential.

Preferably, the discharge initiating scan pulse may have a negative voltage with respect to a reference potential.

Preferably, the method may further include, for a second scan line, c) an address discharge initiating step of initiating a discharge by applying a discharge initiating scan pulse to a scan electrode according to the image data, and an

address pulse having a polarity opposite to that of the discharge initiating scan pulse to an address electrode while the scan pulse is applied; and d) a wall charge accumulating step of applying a wall charge accumulating scan pulse having a polarity opposite to that of the discharge initiating scan pulse and voltage size and width adjustable according to a number of wall charges desired to be accumulated; wherein the discharge initiating scan pulse for the second scan line is applied just after the discharge initiating scan pulse for the first scan line is terminated so as to reduce a total address period for the first and second scan lines.

Preferably, an application interval of the discharge initiating scan pulse for the second scan line may have an interval that is superposed on an application interval of the wall charge accumulating scan pulse for the first scan line.

Brief Description of the Drawings

FIG. 1a is a perspective view showing the structure of a conventional AC type surface-discharge PDP;

FIG. 1b is a plan view showing the structure of the conventional AC type surface-discharge PDP;

FIG. 2a is a driving waveform chart showing waveforms applied to respective electrodes during the driving of a conventional AC PDP;

FIG. 2b is an enlarged waveform chart for a reset period, an address period and a period in the driving waveform chart showing waveforms applied to respective electrodes during the driving of the conventional AC PDP;

FIG. 2c is a diagram showing the behavior of discharges and wall charges for a reset period, an address period and a period for which a single sustain pulse is applied during the driving of the conventional AC PDP;

FIG. 3a is a diagram showing the temporal structure of sub-fields applied to display a single TV screen in the convention AC PDP;

FIG. 3b is a diagram showing the time ratios of respective periods in a

single sub-field in the conventional AC PDP;

FIG. 4 is a waveform chart illustrating the variation of a voltage, a current and infrared rays with time for a single address discharge during the driving of the conventional AC PDP;

FIG. 5 is a diagram showing waveforms that are applied to respective electrodes in the conventional AC PDP, and waveforms that are applied to respective electrodes in accordance with the present invention;

FIG. 6a is a chart showing an example of waveforms applied to the electrodes during the driving of the AC PDP in accordance with the present invention;

FIG. 6b is an enlarged waveform chart for the reset period, the address period and the sustain period in the chart showing waveforms applied to the respective electrodes during the driving of the AC PDP in accordance with the present invention;

FIG. 6c is a diagram showing the behavior of discharges and wall charges for the reset period, the address period and the sustain period during the driving of the AC PDP in accordance with the present invention;

FIG. 7a is a schematic diagram showing the influence of the address discharge of an adjacent scan line in a cell in which a preceding address discharge has been generated in the address period of the AC PDP using the behavior of a discharge and wall charges in accordance with the present invention;

FIG. 7b is a schematic diagram showing the influence of the address discharge of an adjacent scan line in a cell in which a preceding address discharge has not been generated using the behavior of a discharge and wall charges in accordance with the present invention;

FIG. 8a is a diagram showing the temporal structure of sub-fields applied to display a single TV screen in the AC PDP of the present invention;

FIG. 8b is a diagram showing the time ratios of respective periods in a single sub-field in the AC PDP of the present invention; and

FIGS. 9a, 9b, 9c and 9d are waveform charts showing modified

waveforms that can be applied to the respective electrodes to perform high-speed addressing of the AC PDP of the present invention.

<Description of reference numerals of principal elements of the drawings>

1: front substrate	2: back substrate
3: partition wall	4: address electrode
5: fluorescent film	6: transparent electrode
7: bus electrode	8: dielectric layer
9: protective layer	

Best Mode for Carrying Out the Invention

Hereinafter, preferred embodiments of the present invention will be described in detail with reference to the attached drawings. Attention should be paid to the fact that, in attaching reference numerals to the elements of the drawings, the same reference numerals have been used throughout the different drawings to designate the same or similar elements.

FIG. 4 is a waveform chart illustrating the variation of a voltage, a current and infrared rays with time in a single address discharge generated by a scan pulse and an address pulse in a general address process. In FIG. 4, the infrared rays are generated along the same reaction path as VUV rays, so that the variation of the VUV rays with time can be traced using the infrared rays. After a displacement current corresponding to an electric charging flows due to the structural characteristic of the PDP, in which respective electrodes are covered with a dielectric material, in the interval of the introduction of scan and address pulses, an address discharge is generated by the voltage difference between the scan and address pulses, a discharge current flows and infrared rays are emitted in T22. After the address discharge has begun, the discharge is rapidly extinguished by the wall charges accumulated on the respective electrodes. In T23, the space charges that exist after the discharge has been extinguished are

converted into wall charges by a voltage difference continuously applied, and are accumulated. In the falling regions of the scan and address pulses, displacement currents generated due to the structural characteristics of the PDP flow again. When the introduction stage in which the voltages are applied to the respective electrodes, the discharge generation stage and the voltage sustain stage are evaluated in terms of time, these stages occupy 0.3 μs, 0.6 μs and 3 μs.

FIG. 5 shows waveforms that are applied to respective electrodes in a conventional AC PDP, and waveforms that are applied to respective electrodes in accordance with the present invention. Since the discharge and the accumulation of the charges are performed in the same process as described above with reference to FIG. 4, the waveforms applied to the electrodes in the convention AC PDP during the address discharge each have a width of a value more than 0.3 μs so that the sufficient accumulation of the wall charges is achieved to stabilize the sustain discharge. In the present invention, a time for which a designated line occupies the address electrode can be minimally reduced and a time which is required for the address period can be decreased by applying a double voltage having different voltage values and polarities as the scan pulse applied to the scan electrode of the designated line and, therefore, allowing the discharge and the accumulation of the wall charges to be separately performed. Referring to FIG. 5, when the narrow scan pulse is applied through the scan electrode for 0.6 μs that ranges from the generation of the discharge to the extinguishment of the discharge and, at the same time, a pulse having a polarity opposite to that of the scan pulse and a voltage capable of satisfying the condition in which the voltage difference between the scan and address electrodes can trigger the discharge is applied, the address discharge is generated and, at the same time, space charges generated by the discharge are accumulated under the electrodes, so that the discharge is rapidly extinguished. Thereafter, when a pulse of a polarity opposite to that of the pulse applied to the scan electrode is applied for 3 μs, a reverse discharge can be generated by a low voltage through the use of the space charges having been generated and excited particles, and a

complete address process is accomplished by converting the space charges generated by the discharge into wall charges and accumulating the converted wall charges. In this case, about 0.6 μs, which satisfies the condition that the sum of the address and scan pulses can generate the address discharge, is sufficient for the width of the address pulse, and the address pulse can be directly used in the address process of the next scan line, so that the time occupied for the address electrode in a single scan line is reduced from 3 μs to 0.6 μs and the time required to address the entire panel can be reduced to about 1/5 of that of the prior art.

FIG. 6a is an overall driving waveform chart showing waveforms applied to the electrodes X, Y and Z during a single sub-field in the AC PDP in a preferred embodiment of a driving method for performing the high-speed addressing of the present invention. FIG. 6b is an enlarged waveform chart that is plotted for the reset period, the address period and the period for which a single sustain pulse is applied, in accordance with the present invention. FIG. 6c is a diagram showing the behavior of discharges and wall charges during respective intervals divided in the enlarged waveform chart of FIG. 6b.

A detailed description is made with reference to FIGS. 6a, 6b and 6c. T31 is an interval that exhibits the internal state of the discharge space after reset pulses have been applied to the electrodes in the preceding reset period. After the reset period, wall charges hardly exist in the inside of the discharge space, or wall charges are uniformly distributed over the panel. T32 is an interval in which an address discharge is generated due to the voltage difference between the scan electrode Y and the address electrode Z. When a scan pulse a scan pulse having a width of 0.6 μs ranging from the generation of the address discharge to the extinguishments of the discharge is applied to the scan electrode and, at the same time, a pulse having a polarity opposite to that of the scan pulse and having a voltage capable of satisfying the condition in which the voltage difference between the scan and address electrodes can trigger the discharge is applied, space charges generated by the discharge are accumulated under the electrodes at the same time that the address discharge is generated, so that the intensity of an

electric field applied to the inside of the discharge space is reduced and, therefore, the discharge is rapidly extinguished. T33 is an interval in which a reverse discharge is generated by applying a pulse of a polarity opposite to that of the pulse applied to the scan electrode Y. When the pulse is applied for 3 μs, the reverse discharge can be generated between the two sustain electrodes X and Y by a low voltage through the use of the generated space charges or excited particles, and the space charges generated by the discharge are accumulated under the electrodes at the same time that the address discharge is generated, so that the discharge is rapidly extinguished. T34 is an interval in which wall charges are accumulated using the voltage difference between the two sustain electrodes X and Y. In this interval, space charges existing for a certain time after the extinguishment of the discharge in F33 are accumulated under the two sustain electrodes X and Y. T35 is an interval that exhibits the internal state of the discharge space after the address discharge and the accumulation of wall charges. In this interval, after voltages applied to the electrodes to generate the address discharge die out, the accumulated wall charges maintain the state thereof in which the wall charges are accumulated under the electrodes. T36 is an interval in which a sustain pulse is applied through the sustain electrode Y and, consequently, a sustain discharge is generated. In this interval, when a voltage of the same polarity as that of the accumulated wall charges is applied between two sustain electrodes X and Y, the sustain discharge is generated and charges of a polarity opposite to that of the applied voltage begin to be accumulated, so that the discharge is extinguished. T37 is an interval in which space charges are converted into wall charges using an electric field generated by the voltage difference between the two sustain electrodes X and Y. In this interval, the space charges that exist after the discharge has been extinguished are allowed to be accumulated under the two sustain electrodes X and Y. T38 is an interval that exhibits the internal state of the discharge space after the sustain discharge and the accumulation of the wall charges. In this interval, after voltages applied to the electrodes to generate the sustain discharge die out, the accumulated wall

charges maintain the state thereof in which the wall charges are accumulated under the electrodes, and will be used for the next discharge.

In that case, since 0.6 μs, which is the condition to generate the address discharge in T32 of FIG. 6b, is sufficient for the time required to address a single scan line, the address electrode can be used in the address process of the next address line, through which the time required for the address period of a single sub-field can be considerably reduced. As a result, the time required to address the entire panel in a single sub-field 480×0.6 μs+3 μs=0.291 ms in the case of a PDP supporting VGA-level resolution (640×480).

FIGS. 7a and 7b are diagrams showing the influence of the address discharge of an adjacent scan line during the address period of the AC PDP in accordance with the present invention using the behavior of a discharge and wall charges. FIG. 7a is a schematic diagram showing the influence of the address discharge of the adjacent scan line in a cell in which a preceding address discharge has been generated. When an address discharge is generated on a first scan line Line 1 in T41, and a reverse discharge is generated on the first scan line Line 1 and another address discharge is generated on a second scan line Line 2 in T42, the maximum difference between voltages applied to the electrodes on the first scan line Line 1, which is not a designated scan line, during T41 is VA, thus preventing the problem of an erroneous discharge, and the maximum difference between voltages applied on the second scan line Line 1, which is not a designated scan line, during T42 is VO, so that a reverse discharge generated between the two sustain electrodes X and Y is not considerably influenced by a voltage applied to the address voltage Z, thus generating a stable discharge. FIG. 7b is a schematic diagram showing the influence of the address discharge of an adjacent scan line in a cell in which a preceding address discharge has not been generated. When an address discharge is not generated on the first scan line Line 1 in T51, and an address discharge is generated on the second scan line Line 2 in T52, the maximum difference between voltages applied on the first scan line Line 1, which is not a designated scan line, is VO-VA, thus preventing the

problem of an erroneous discharge.

FIG. 8a is a diagram showing waveforms applied for a single TV field (16.67 ms) during the driving of the PDP of the present invention with respect to respective periods. FIG. 8b is a diagram showing times required with respect to respective periods for a single TV field. When the PDP of the present invention having VGA-level resolution is driven using eight sub-fields, the time required for the reset period in a single sub-field is about 0.3 ms, the time required for the address period is about 0.291 ms, the time required for the sustain period is 47 μs to 5.99 ms depending upon designated luminance. Accordingly, as shown in FIG. 8b, in a single field, the reset period occupies 14%, the address period occupies 14% and the sustain period occupies 72%, so that the time required for the address period decreases to 1/5 and the time required for the sustain period increases four times compared to the conventional PDP driving method, thus considerably contributing to the increase of the luminance of the PDP. In particular, when a PDP having Extended Graphics Array (XGA)-level resolution (1024×768) corresponding to a High Definition TV (HDTV) is driven, the time required for the reset period is about 300 μs and the time required for the address period is 768×0.6 μs+3 μs=0.291 ms in a single sub-field, so that the sum of the times required for the reset and address periods is 6.11 ms in a single TV field. Accordingly, since a time of more than 10 ms out of a single TV field time of 16.67 ms can be assigned to a light emitting period, the driving of the PDP is sufficiently enabled. Further, in the case where twelve sub-fields are employed in order to reduce various problems in image quality that occur in a general PDP, the sustain period more than 9.5 ms can be assured, so that stable luminance can be secured.

FIGS. 9a, 9b, 9c and 9d are diagrams showing embodiments using various modifications of waveforms applied to the scan and address electrodes in a driving method of performing a high-speed address process, which is derived from the same inventive concept as the above-described embodiment. FIG. 9a is a diagram showing a modified embodiment including the step of generating a

full-scale address discharge so that wall charges are uniformly accumulated or excited particles are generated to reduce the size of a necessary voltage to be applied to trigger the address discharge in the address process, in the reset process prior to the address period. FIG. 9b is a diagram showing a modified embodiment that is constructed to have a short pause period ranging from the application of a discharge initiating scan pulse before the application of a wall charge accumulating scan pulse to prevent an erroneous discharge that can be generated by the rapid voltage variation of the scan pulse. FIG. 9c is a diagram indicating that the present invention can be properly modified to generate the same function as the above-described embodiment even though the polarity of the scan and address pulses varies. FIG. 9d is a diagram showing another modified embodiment including the step of maintaining a certain-sized voltage other than a reference potential on a command sustain electrode X in the address process.

As described above, although the specific embodiments have been described above, various modifications are possible without departing from the scope of the invention as a matter of course. Accordingly, the scope of the present invention is not limited to the above-described embodiments, but should be determined by equivalents for the attached claims as well as the attached claims.

Industrial Applicability

In accordance with the present invention, the time for which a designated scan line occupies an address electrode is minimally reduced and the time required to address an entire panel is reduced by dividing a discharge initiating interval and a wall charge accumulating interval using two scan pulses in the address period, so that a light emission time is lengthened in a single TV field. Accordingly, there can be provided the driving method in which the luminance of the AC PDP is improved, the AC PDP having XGA-level resolution can be allowed to be stably driven without changing the structure thereof, and reduced

luminance due to the reduction of the light emission time can be compensated for when the number of sub-fields is increased to improve image quality, thus being capable of implementing a high image quality PDP.

Claims

1. A method of driving an Alternating Current (AC) Plasma Display Panel (PDP) in an address period to write image data, the AC PDP having a plurality of discharge cells for implementing images and a plurality of scan and address electrodes (Y and Z) for controlling the discharge cells, comprising, for a first line:

a) an address discharge initiating step of initiating a discharge by applying a discharge initiating scan pulse to a scan electrode according to the image data, and an address pulse having a polarity opposite to that of the discharge initiating scan pulse to an address electrode while the scan pulse is applied; and

b) a wall charge accumulating step of applying a wall charge accumulating scan pulse having a polarity opposite to that of the discharge initiating scan pulse and voltage size and width adjustable according to a number of wall charges desired to be accumulated.

2. The method as set forth in claim 1, wherein the wall charge accumulating scan pulse has a voltage lower than the discharge initiating scan pulse.

3. The method as set forth in claim 1, wherein the wall charge accumulating scan pulse is applied when a certain pause period elapses after the application of the discharge initiating scan pulse.

4. The method as set forth in claim 1, further comprising the step of maintaining a certain voltage on a common sustain electrode (X) during a partial interval of the address period.

5. The method as set forth in claim 1, further comprising the step of generating a full-scale address discharge in a reset period prior to the address

period to reduce necessary voltage of pulses applied to the electrodes in the address period.

6. The method as set forth in claim 1, wherein the discharge initiating scan pulse has a positive voltage with respect to a reference potential.

7. The method as set forth in claim 1, wherein the discharge initiating scan pulse has a negative voltage with respect to a reference potential.

8. The method as set forth in claim 1, further comprising, for a second scan line:

c) an address discharge initiating step of initiating a discharge by applying a discharge initiating scan pulse to a scan electrode according to the image data, and an address pulse having a polarity opposite to that of the discharge initiating scan pulse to an address electrode while the scan pulse is applied; and

d) a wall charge accumulating step of applying a wall charge accumulating scan pulse having a polarity opposite to that of the discharge initiating scan pulse and voltage size and width adjustable according to a number of wall charges desired to be accumulated;

wherein the discharge initiating scan pulse for the second scan line is applied just after the discharge initiating scan pulse for the first scan line is terminated so as to reduce a total address period for the first and second scan lines.

9. The method as set forth in claim 8, wherein an application interval of the discharge initiating scan pulse for the second scan line has an interval that is superposed on an application interval of the wall charge accumulating scan pulse for the first scan line.

Fig. 1a

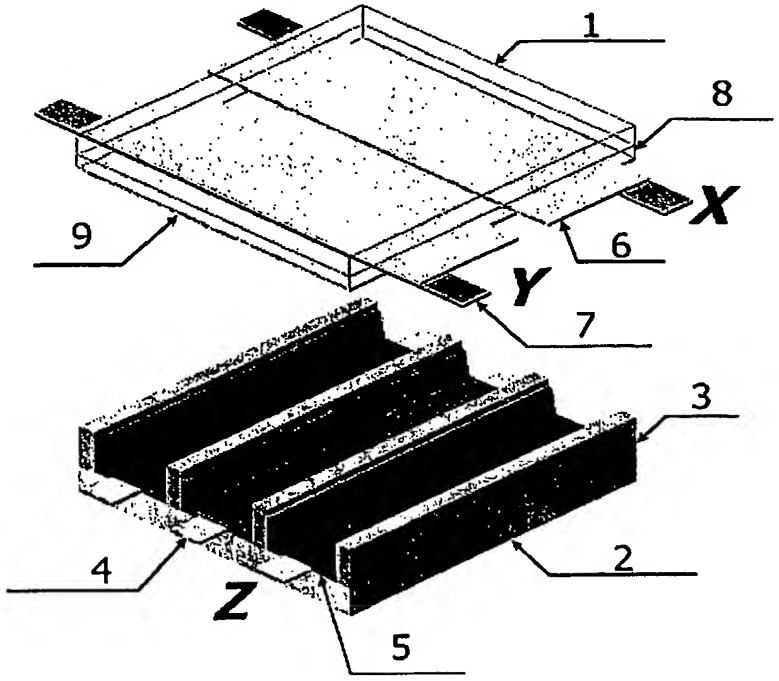


Fig. 1b

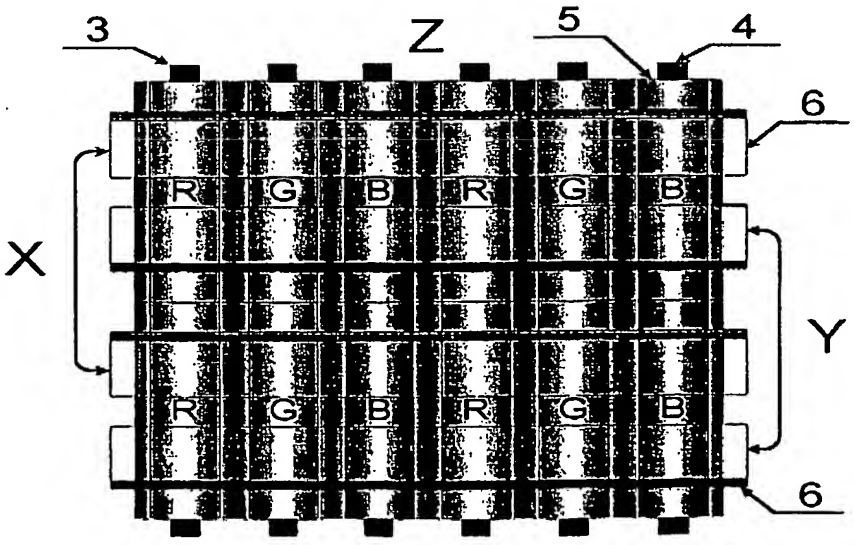


Fig. 2a

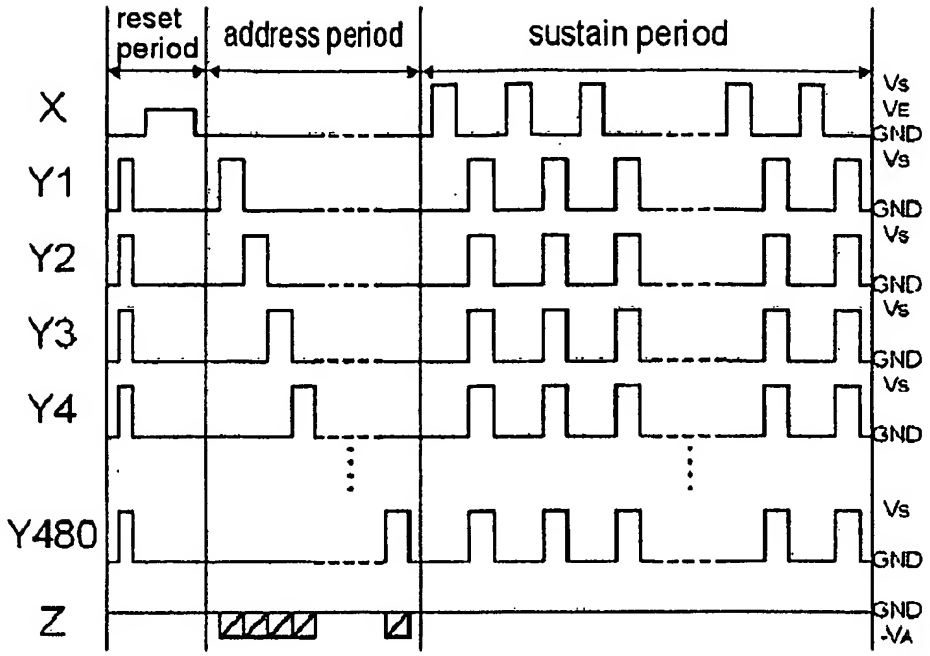

reset period
address period
sustain period
X
Y1
Y2
Y3
Y4
Y480
Z
Vs
VE
GND
-VA

Fig. 2b

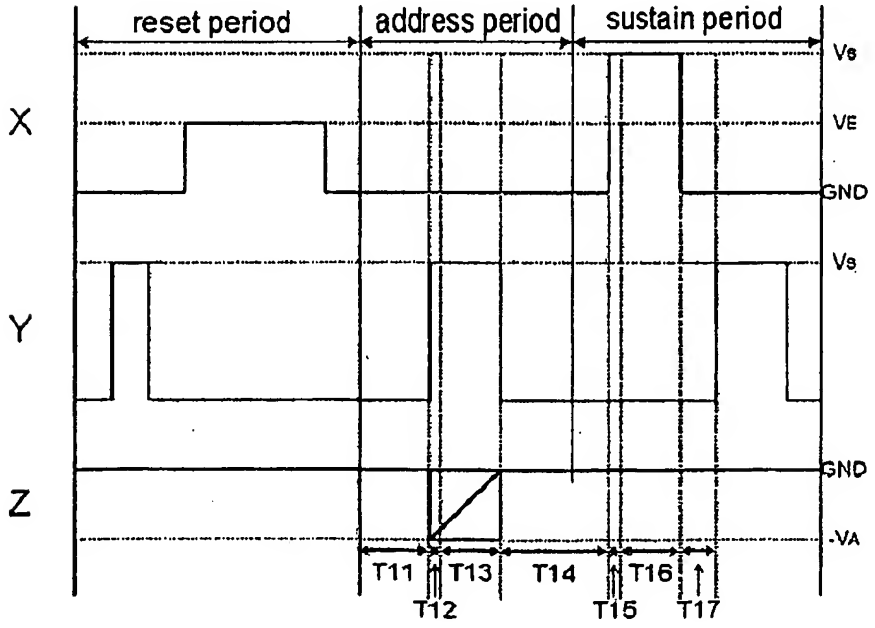

reset period
address period
sustain period
X
Y
Z
Vs
VE
GND
-VA
T11
T12
T13
T14
T15
T16
T17

Fig. 2c

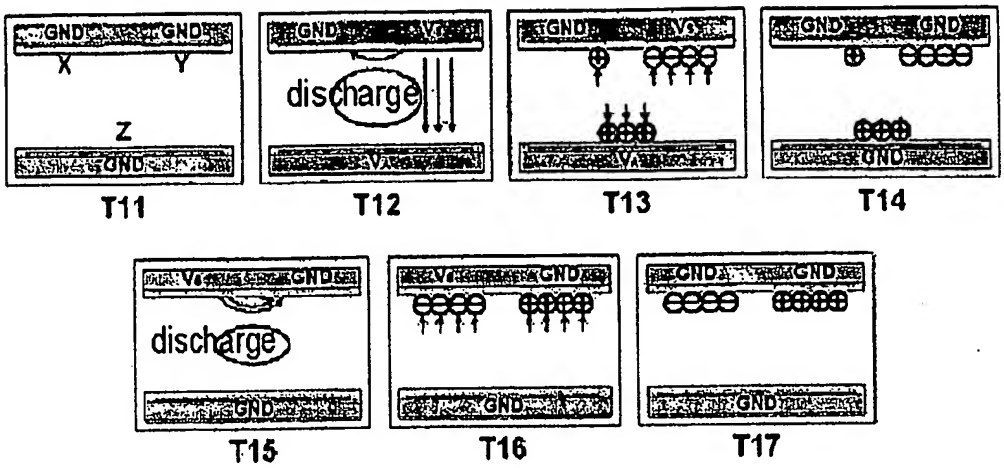


Fig. 3a

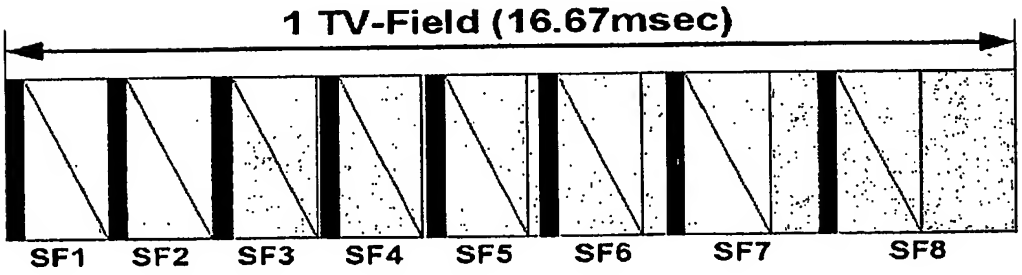


Fig. 3b

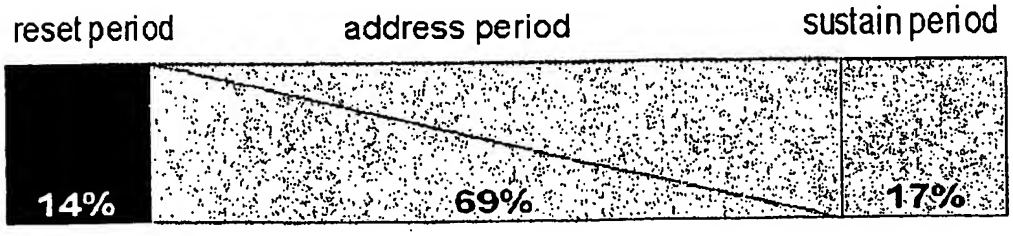


Fig. 4

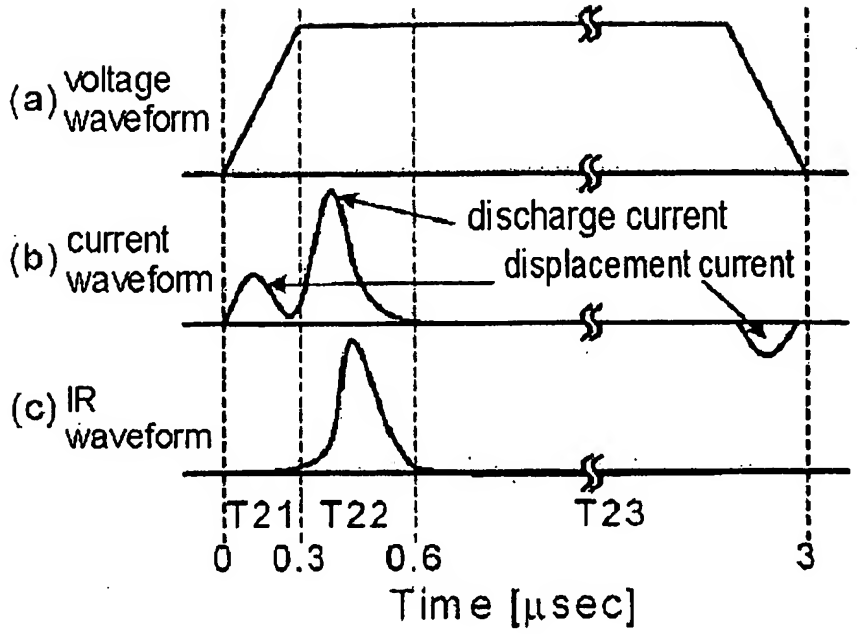

(a) voltage waveform
(b) current waveform
discharge current
displacement current
(c) IR waveform
T21
T22
T23
0
0.3
0.6
3
Time [μsec]

Fig. 5

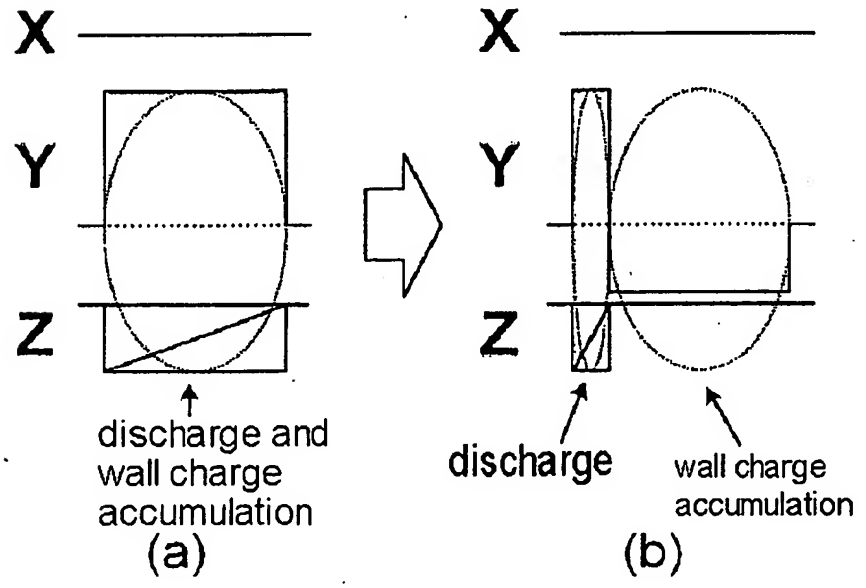

X
Y
Z
discharge and wall charge accumulation
(a)
X
Y
Z
discharge
wall charge accumulation
(b)

Fig. 6a

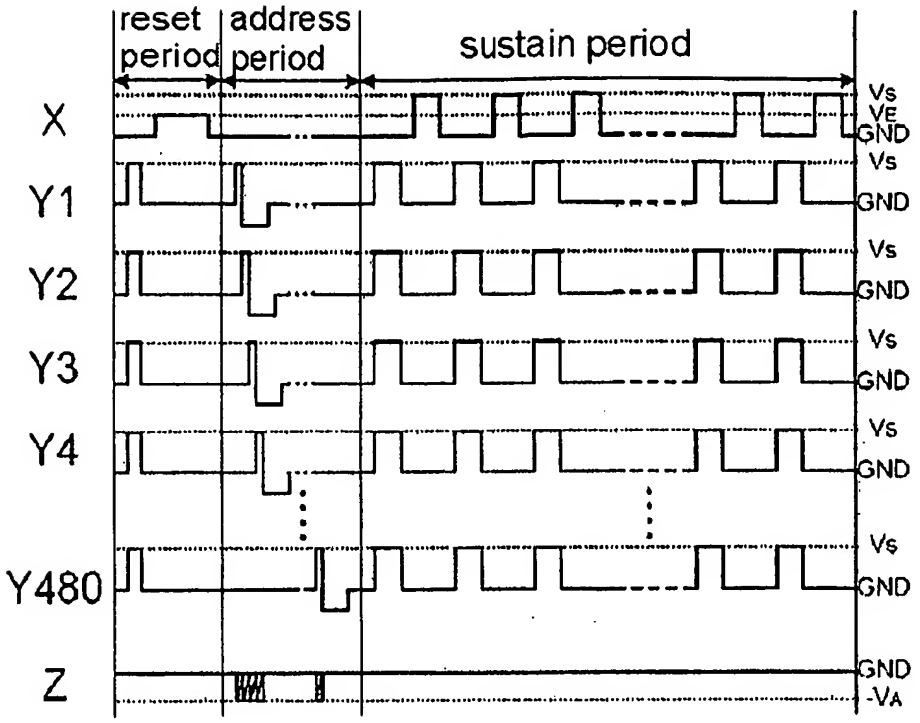

reset period
address period
sustain period
X
Y1
Y2
Y3
Y4
Y480
Z
Vs
VE
GND
-VA

Fig. 6b

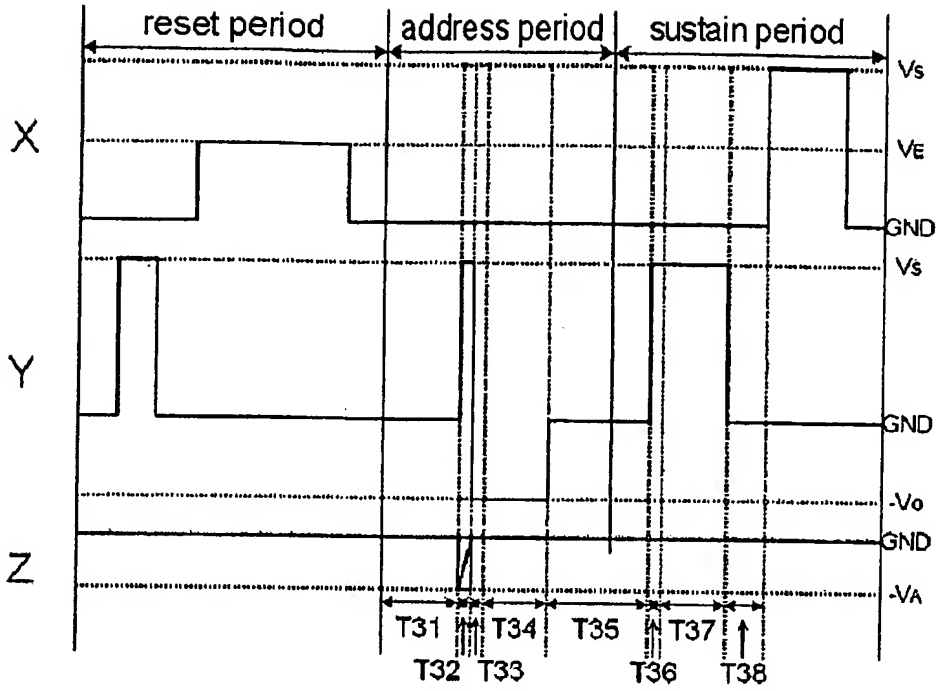

reset period
address period
sustain period
X
Y
Z
Vs
VE
GND
Vs
GND
-Vo
GND
-VA
T31
T32
T33
T34
T35
T36
T37
T38

Fig. 6c

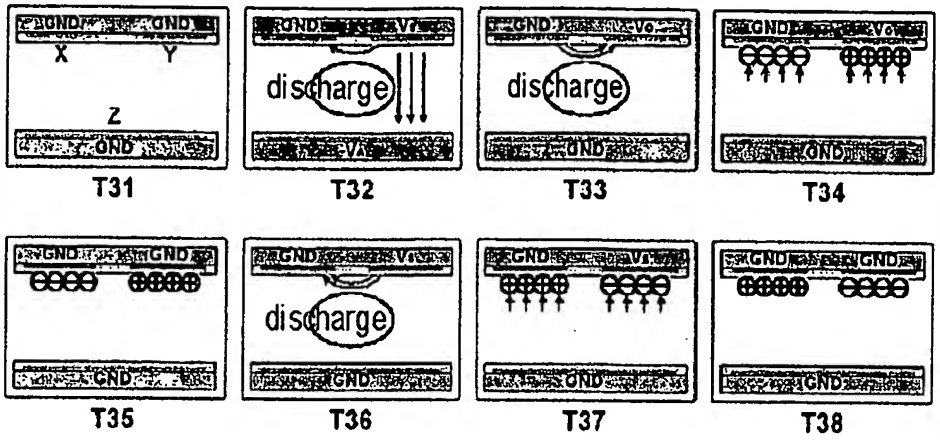

GND
X
Y
Z
discharge
T31
T32
T33
T34
T35
T36
T37
T38

Fig. 7a

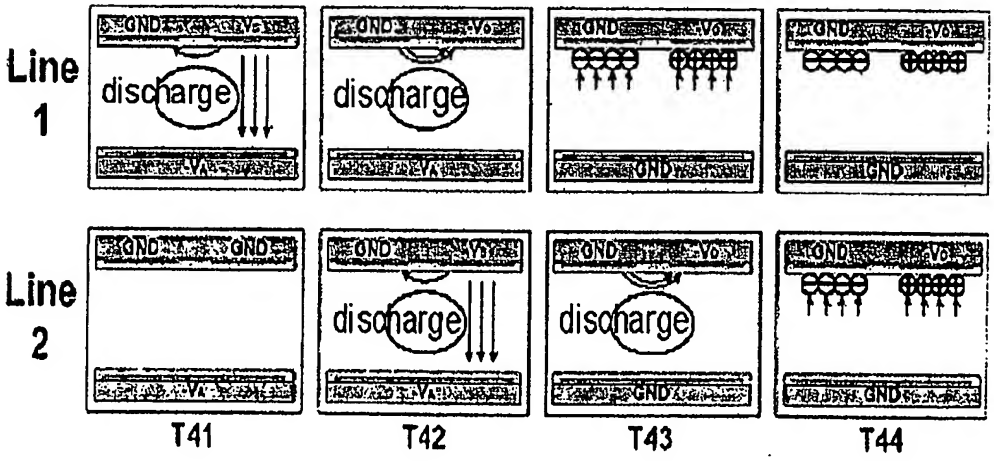

Line 1
Line 2
discharge
GND
T41
T42
T43
T44

Fig. 7b

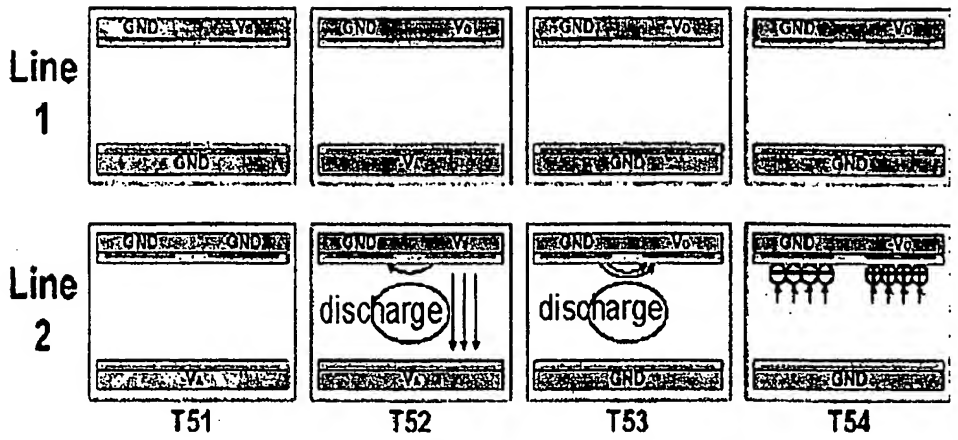

Line 1
Line 2
GND
Vo
discharge
T51
T52
T53
T54

Fig. 8a

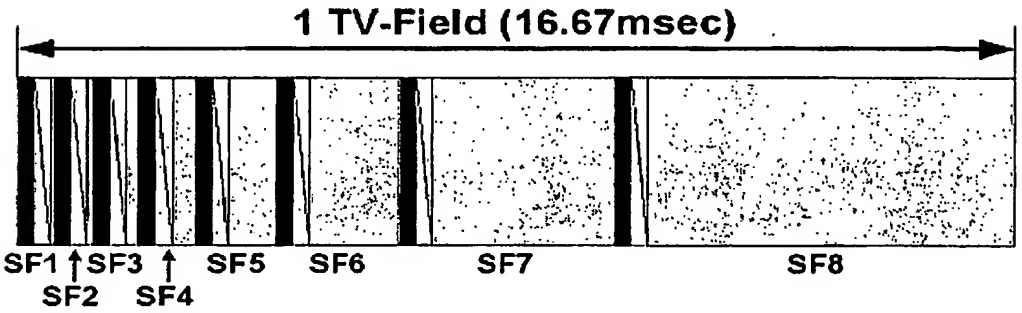

1 TV-Field (16.67msec)
SF1
SF2
SF3
SF4
SF5
SF6
SF7
SF8

Fig. 8b

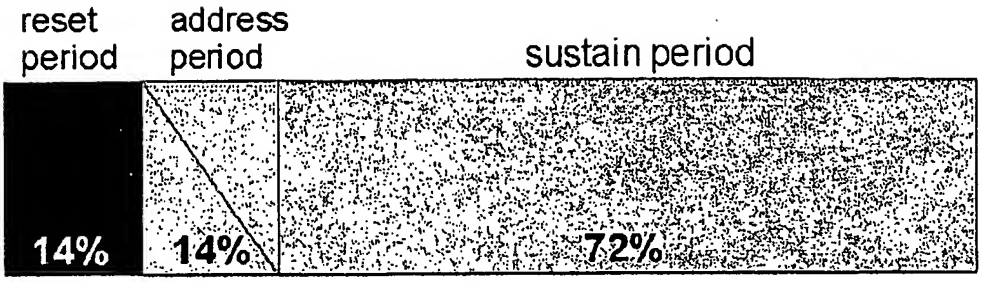

reset period
address period
sustain period
14%
14%
72%

Fig. 9a

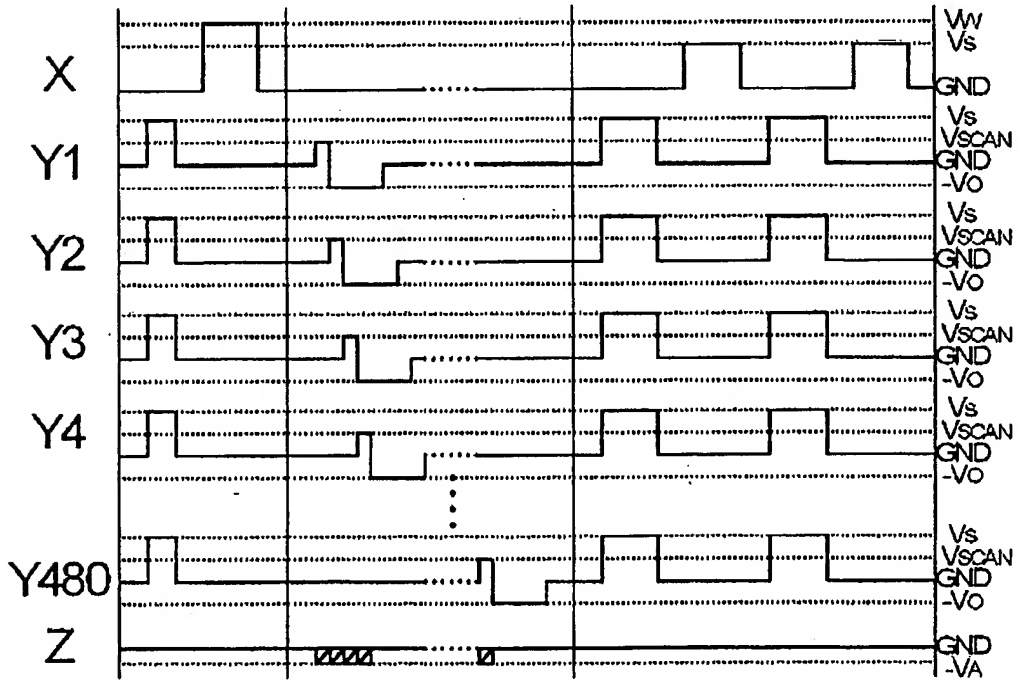

X
Y1
Y2
Y3
Y4
Y480
Z
Vw
Vs
GND
Vs
VSCAN
GND
-Vo
Vs
VSCAN
GND
-Vo
Vs
VSCAN
GND
-Vo
Vs
VSCAN
GND
-Vo
Vs
VSCAN
GND
-Vo
GND
-VA

Fig. 9b

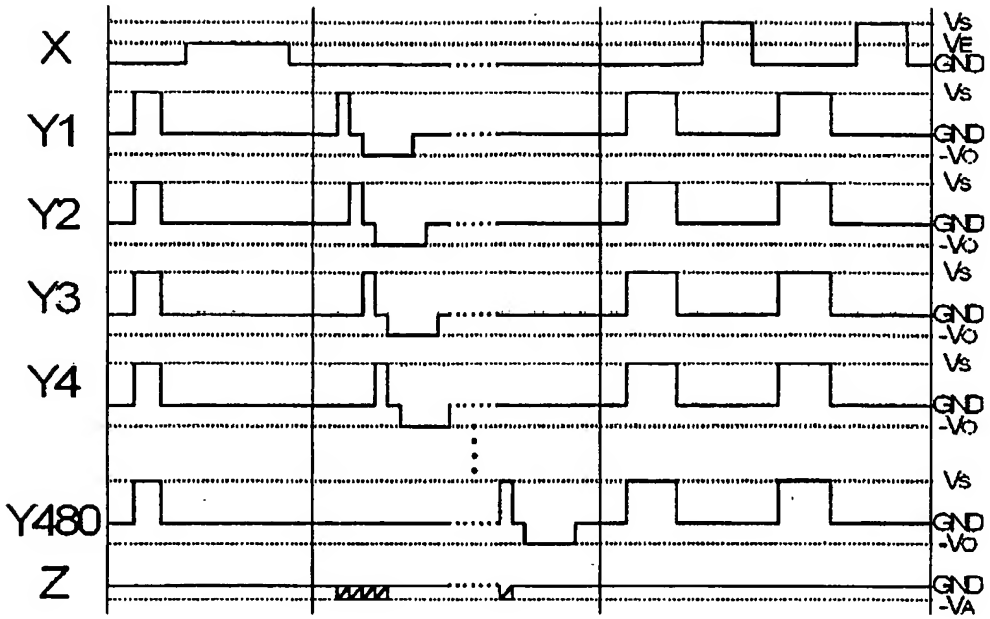

X
Y1
Y2
Y3
Y4
Y480
Z
Vs
VE
GND
-Vo
-VA

Fig. 9c

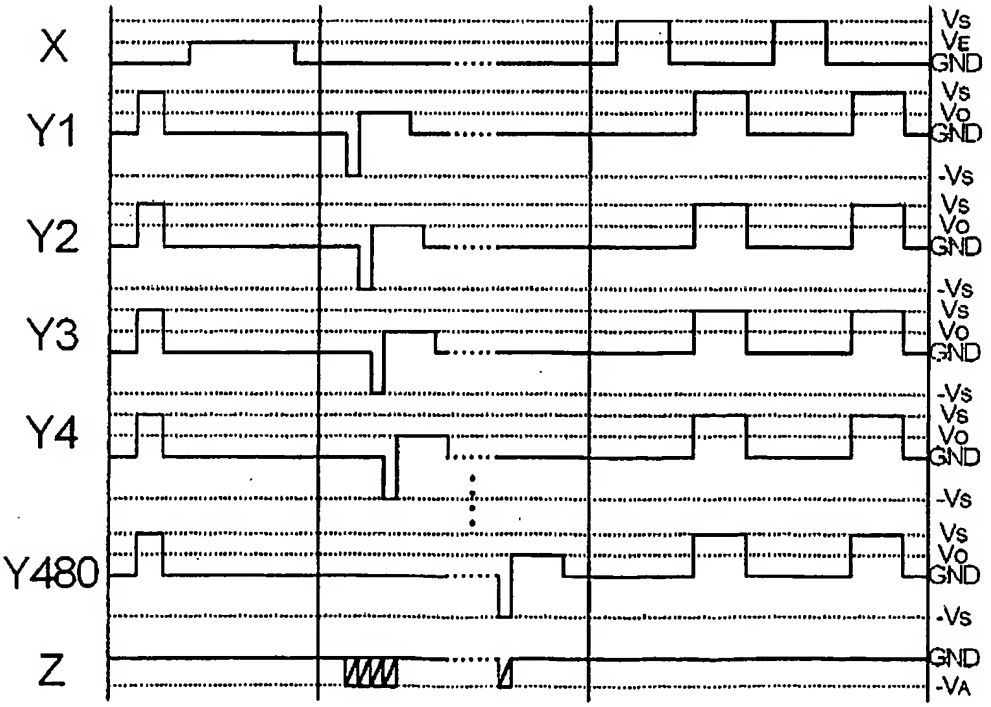
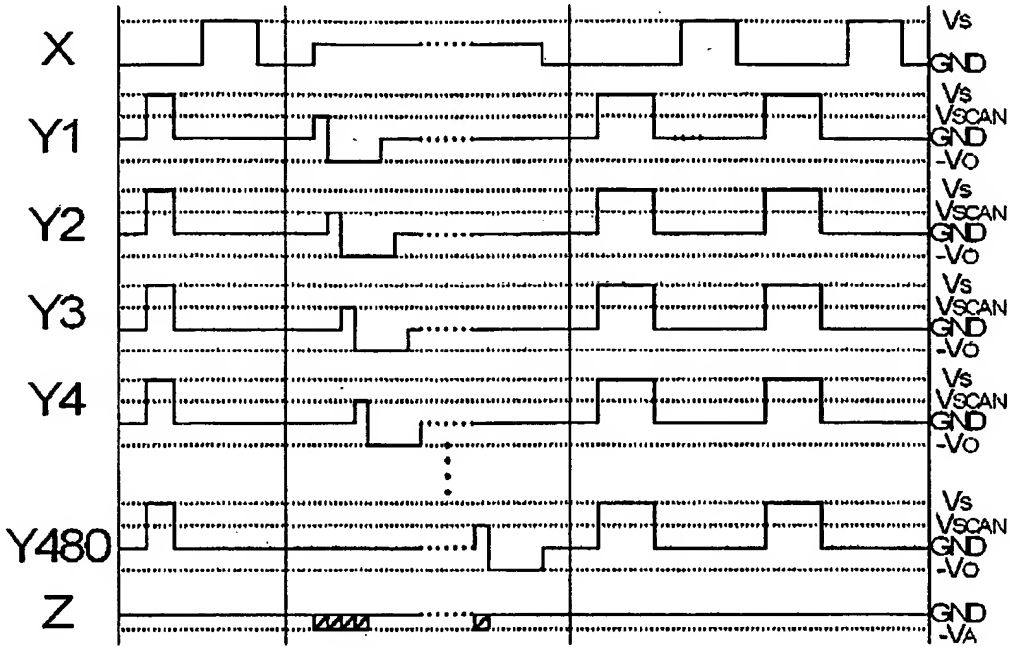

X
Y1
Y2
Y3
Y4
Y480
Z
Vs
VE
GND
Vo
-Vs
-VA

Fig. 9d


X
Y1
Y2
Y3
Y4
Y480
Z
Vs
GND
Vs
VSCAN
GND
-Vo
Vs
VSCAN
GND
-Vo
Vs
VSCAN
GND
-Vo
Vs
VSCAN
GND
-Vo
Vs
VSCAN
GND
-Vo
GND
-VA

INTERNATIONAL SEARCH REPORT

international application No.
PCT/KR03/00987

A. CLASSIFICATION OF SUBJECT MATTER

IPC7 G09G 3/288

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G09G3/28 - 3/288

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
KR, JP as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
FPD, PAJ, USPAT

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
PA	JP 2002- 351398 A (Matsushita Electric IND CO LTD) 6 DEC 2002 See abstract and Fig.1	1
A	JP 2002-72960 A ((Matsushita Electric IND CO LTD) 12 May 2002 See abstract and Fig.1	1
A	EP 1022713 A (NEC Corporation) 26 JUL 2000 See abstract and Fig.5A - 5E	1

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
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Date of the actual completion of the international search	Date of mailing of the international search report
01 SEPTEMBER 2003 (01.09.2003)	01 SEPTEMBER 2003 (01.09.2003)

Name and mailing address of the ISA/KR	Authorized officer
Korean Intellectual Property Office 920 Dunsan-dong, Seo-gu, Daejeon 302-701, Republic of Korea Facsimile No. 82-42-472-7140	JEONG, Jae Heon Telephone No. 82-42-481-5672

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/KR03/00987

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
JP 2002-351398 A	06/12/2002	NONE	
JP 2002-72960 A	12/03/2002	NONE	
EP 1022713 A	26/07/2000	US 6573878 A JP 2000-206933 A	03/06/2003 08/09/2000

Form PCT/ISA/210 (patent family annex) (July 1998)